

Description

N-channel Enhancement Mode Power MOSFET

Features

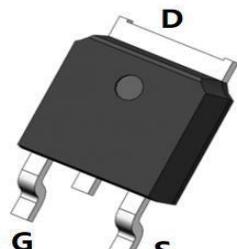
- 100V, 15A
- $R_{DS(ON)} < 108\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
- $R_{DS(ON)} < 125\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low GateCharge

Applications

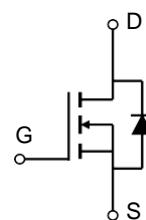
- Load Switch
- PWM Application
- Power Management



100% UI TESTED!
100% ΔVds TESTED!



TO-252-3L



Schematic Diagram

Package Marking and Ordering Information

DeviceMarking	Device	Outline	Package	ReelSize	Reel(pcs)	PerCarton (pcs)
OCT10N10K	OCT10N10K	TAPING	TO-252-3L	13"	2500	25000

Absolute Maximum Ratings(@ $T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Value		Units	
V_{DS}	Drain-to-Source Voltage		100		V	
V_{GS}	Gate-to-Source Voltage		± 20		V	
I_D	Continuous Drain Current	$T_c=25^\circ\text{C}$	15		A	
		$T_c=100^\circ\text{C}$	9			
I_{DM}	Pulsed Drain Current ⁽¹⁾		60		A	
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾		6		mJ	
P_D	Power Dissipation	$T_c=25^\circ\text{C}$	44		W	
$R_{\theta JC}$	Thermal Resistance ,Junction to Case		3		$^\circ\text{C}/\text{W}$	
T_J, T_{STG}	Junction & Storage Temperature Range		-55 to 150		$^\circ\text{C}$	

Electrical Characteristics($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm20\text{V}$	-	-	±100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$R_{DS(\text{ON})}$	Static Drain-Source ON-Resistance ⁽³⁾	$V_{GS}=10\text{V}, I_D=5\text{A}$	-	86.0	108.0	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=3\text{A}$	-	96.0	125.0	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1\text{MHz}$	-	847	-	pF
C_{oss}	Output Capacitance		-	40	-	pF
C_{rss}	Reverse Transfer Capacitance		-	12	-	pF
Q_g	Total Gate Charge	$V_{GS}=0\text{to}10\text{V}$ $V_{DS}=50\text{V}, I_D=2\text{A}$	-	20	-	nC
Q_{gs}	Gate Source Charge		-	2.8	-	nC
Q_{gd}	Gate Drain("Miller")Charge		-	4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DD}=50\text{V}$ $I_D=3\text{A}, R_{GEN}=1.8\Omega$	-	6	-	ns
t_r	Turn-On Rise Time		-	7	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	21	-	ns
t_f	Turn-Off Fall Time		-	3	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	15	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	60	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_S=10\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=10\text{A}, di/dt=100\text{A}/\mu\text{s}$	-	22	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	29	-	nC

Notes:

- 1.Repetitive Rating:Pulse Width Limited by Maximum Junction Temperature.

2. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=50\text{V}, V_G=10\text{V}, L=0.5\text{mH}, R_g=25\Omega, I_{AS}=5\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

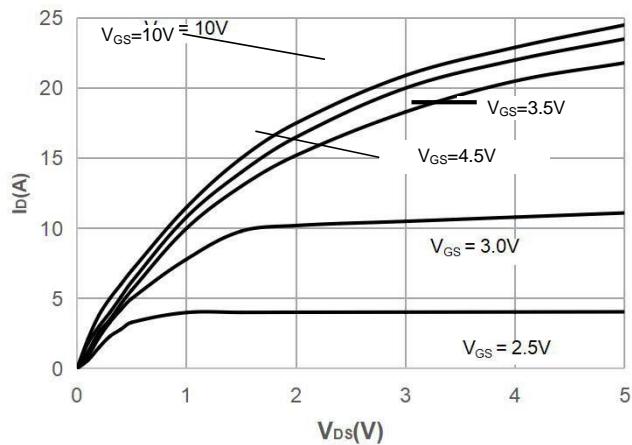


Figure 2: Typical Transfer Characteristics

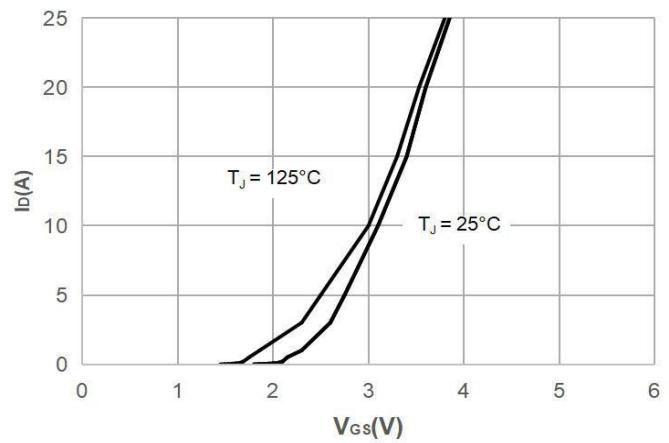


Figure 3: On-resistance vs. Drain Current

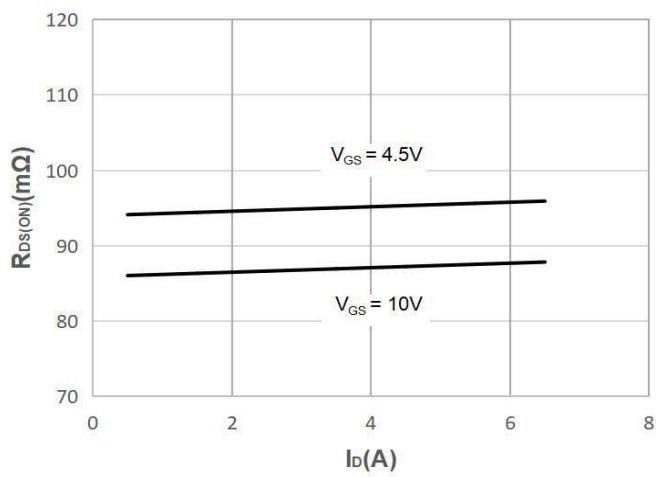


Figure 4: Body Diode Characteristics

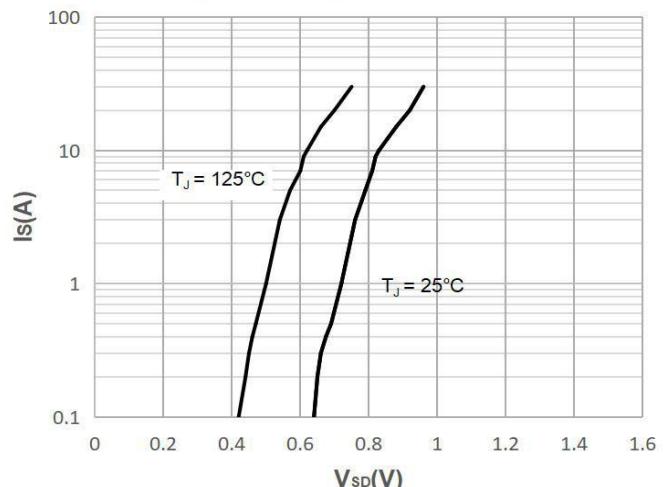


Figure 5: Gate Charge Characteristics

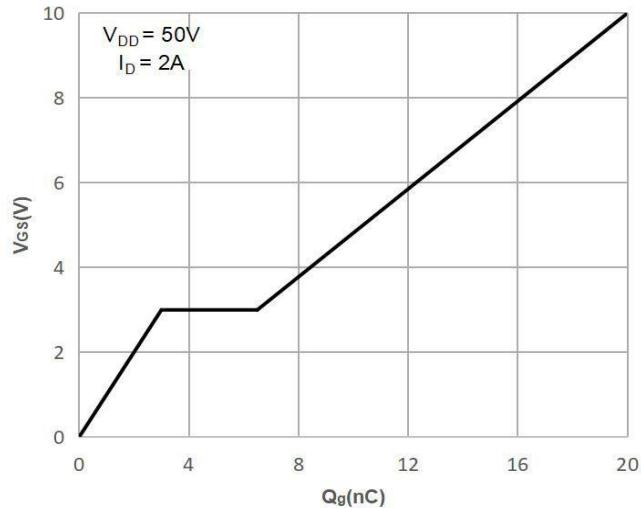
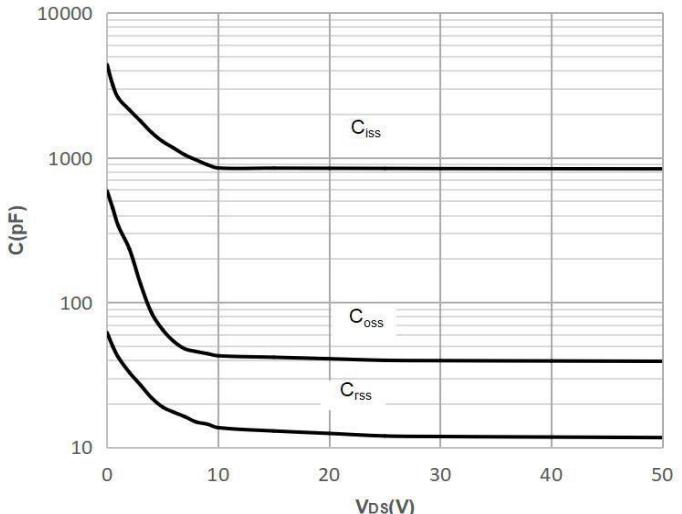


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

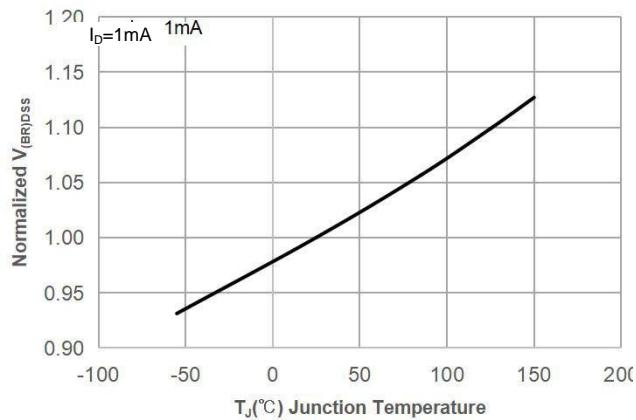


Figure 8: Normalized on Resistance vs. Junction Temperature

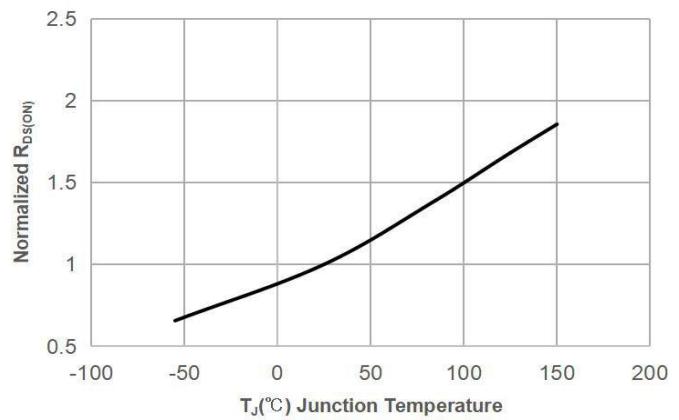


Figure 9: Maximum Safe Operating Area

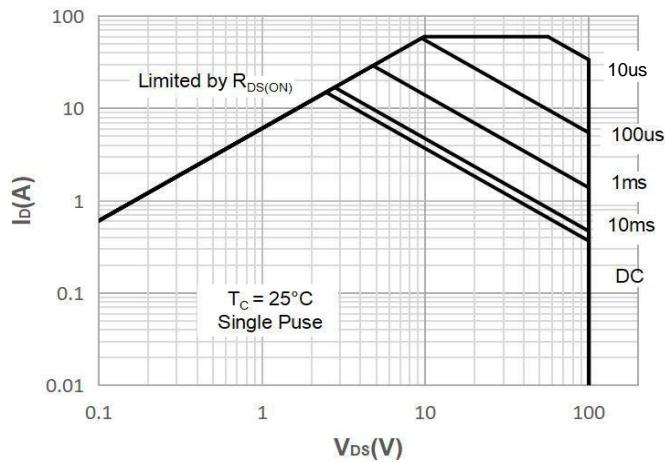


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

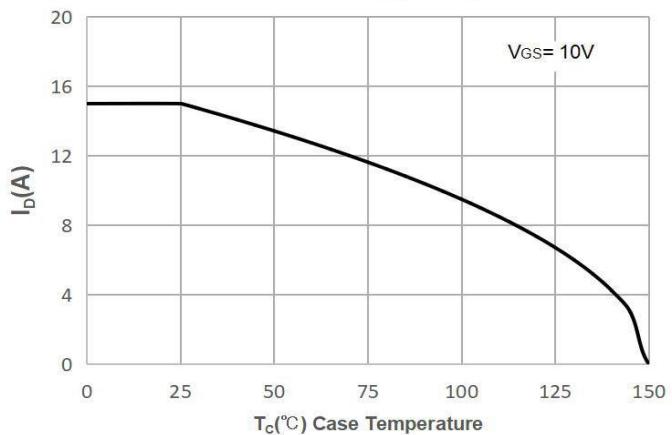


Figure 11: Normalized Maximum Transient Thermal Impedance

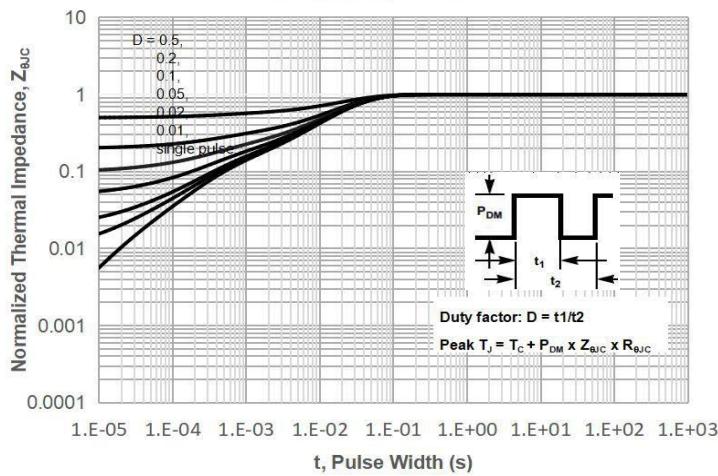
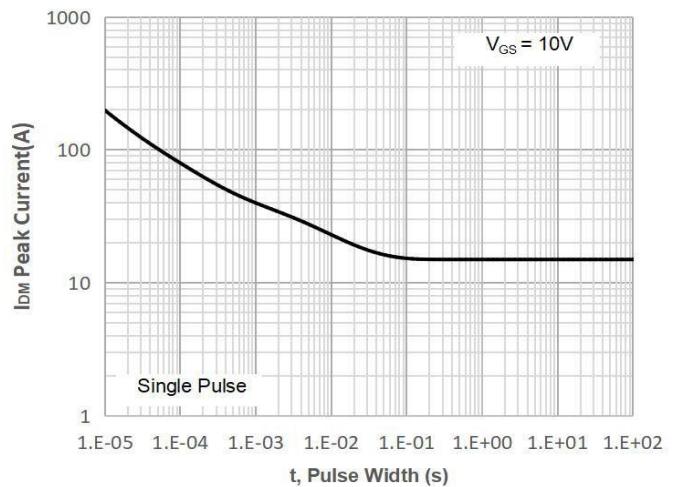


Figure 12: Peak Current Capacity



Test Circuit

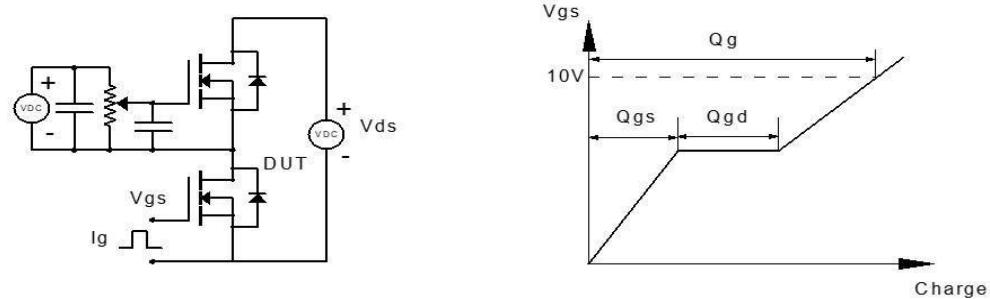


Figure1:GateChargeTestCircuit&Waveform

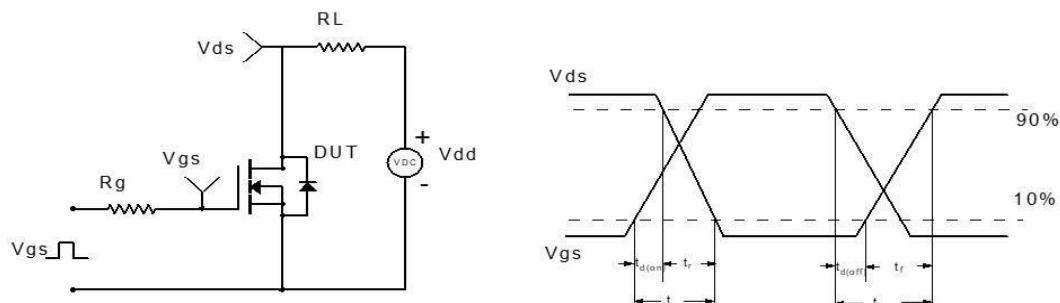


Figure2:ResistiveSwitchingTestCircuit&Waveform

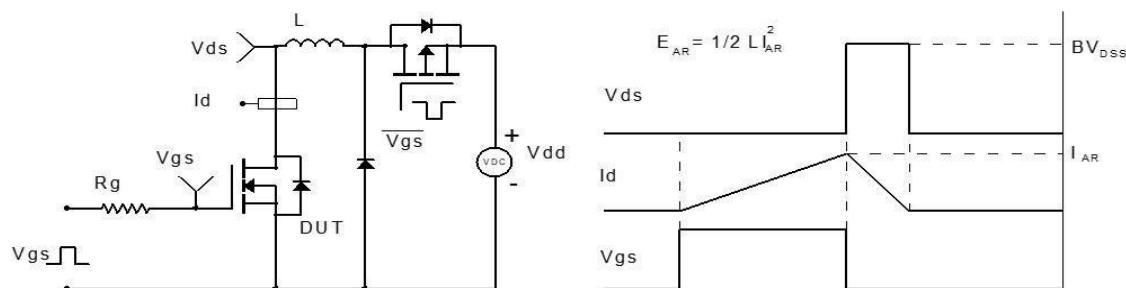


Figure3:UnclampedInductiveSwitchingTestCircuit&Waveform

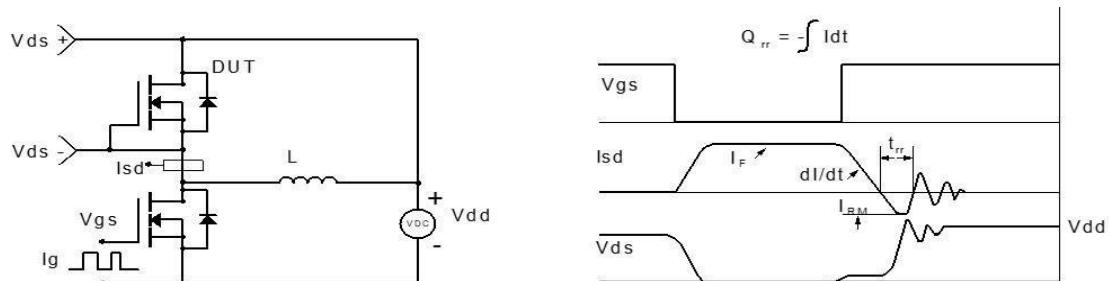
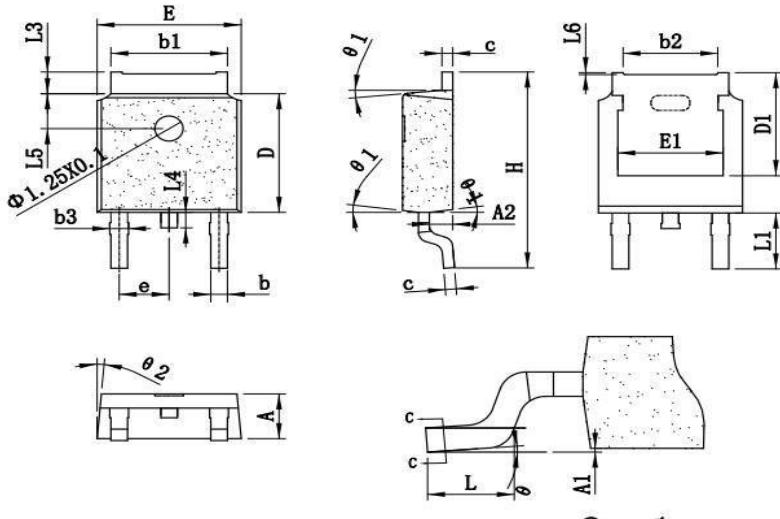


Figure4:DiodeRecoveryTestCircuit&Waveform

Package Mechanical Data(TO-252-3L)



SYMBOL	mm		
	MIN	NOM	MAX
*A	2.20	2.30	2.38
*A1	0.00	—	0.15
*A2	0.90	1.00	1.10
*b	0.72	0.78	0.85
b1	5.23	5.33	5.46
b2	4.05	4.20	4.35
*b3	0.78	0.85	0.90
*c	0.47	0.52	0.55
*D	6.00	6.10	6.20
D1	5.40REF		
*E	6.50	6.60	6.70
E1	4.70	4.83	4.92
*e	2.286BSC		
*H	9.90	10.10	10.20
*L	1.40	1.55	1.70
L1	2.90REF		
L3	0.90	—	1.20
L4	0.75	0.85	0.95
L5	1.70	1.80	1.90
L6	0.00	0.06	0.12
*θ	0°	—	5°
θ1	5°	7°	9°
θ2	5°	7°	9°