

## Description

### N-channel Enhancement Mode Power MOSFET

#### Features

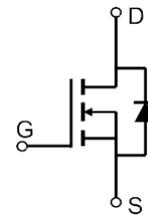
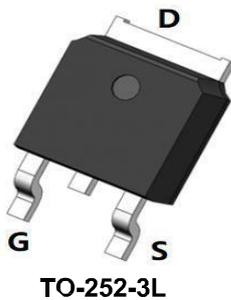
- 60V, 30A  
 $R_{DS(ON)} < 33m\Omega @ V_{GS} = 10V$  (TYP. 26m $\Omega$ )  
 $R_{DS(ON)} < 45m\Omega @ V_{GS} = 4.5V$  (TYP. 33m $\Omega$ )
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge

#### Applications

- Load Switch
- PWM Application
- Power Management



!  
100%  $\Delta V_{ds}$  TESTED!



Schematic Diagram

### Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
30N06K	OCT30N06K	TAPING	TO-252-3L	13"	2500	25000

### Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

$V_{DS}$	Drain-to-Source Voltage		60	V
$V_{GS}$	Gate-to-Source Voltage		$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ\text{C}$	30	A
		$T_C = 100^\circ\text{C}$	19	
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>		100	
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(2)</sup>		27	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	28	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		5.4	
$T_J, T_{STG}$	Junction & Storage Temperature Range		-55 to 150	$^\circ\text{C}$

**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.6	2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = 10\text{V}, I_D = 10\text{A}$	-	26	33	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$	-	33	45	$\text{m}\Omega$
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1\text{MHz}$	-	860	-	pF
$C_{oss}$	Output Capacitance		-	62	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	51	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 30\text{V}, I_D = 10\text{A}$	-	20.3	-	nC
$Q_{gs}$	Gate Source Charge		-	3.7	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge		-	5.3	-	nC
$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 30\text{V}$ $I_D = 20\text{A}, R_{GEN} = 1.8\Omega$	-	7.6	-	ns
$t_r$	Turn-On Rise Time		-	20	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	15	-	ns
$t_f$	Turn-Off Fall Time		-	24	-	ns
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	30	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	100	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 15\text{A}$	-	-	1.2	V

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
  2.  $E_{AS}$  condition: Starting  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 30\text{V}$ ,  $V_G = 10\text{V}$ ,  $R_G = 25\text{ohm}$ ,  $L = 0.5\text{mH}$ ,  $I_{AS} = 10.5\text{A}$
  3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$

## Typical Performance Characteristics

Figure 1: Output Characteristics

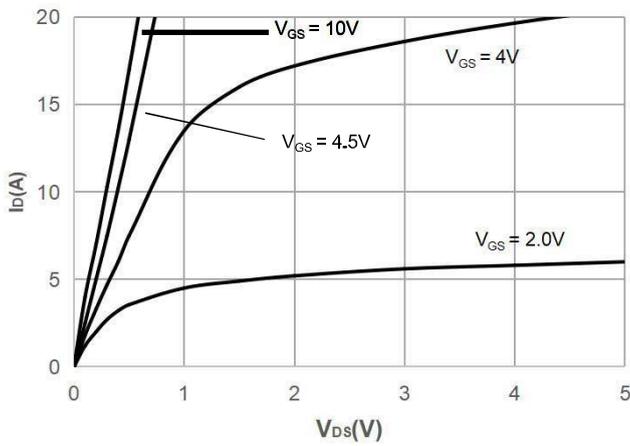


Figure 2: Typical Transfer Characteristics

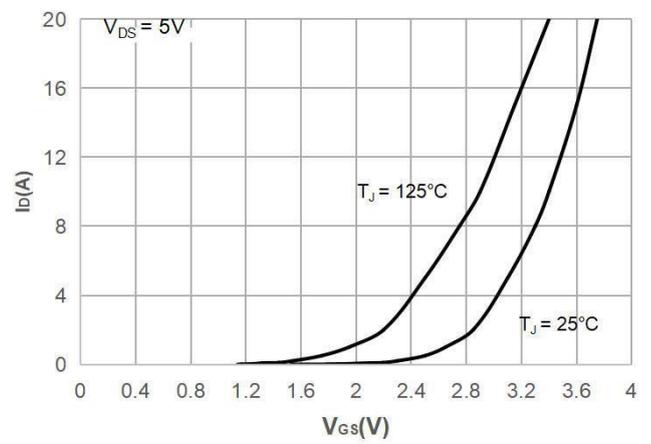


Figure 3: On-resistance vs. Drain Current

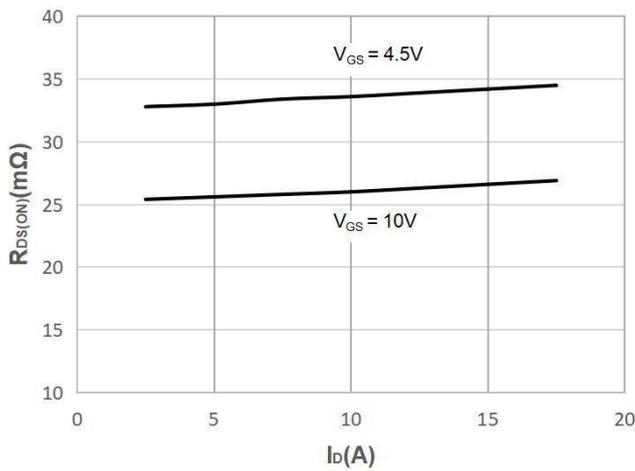


Figure 4: Body Diode Characteristics

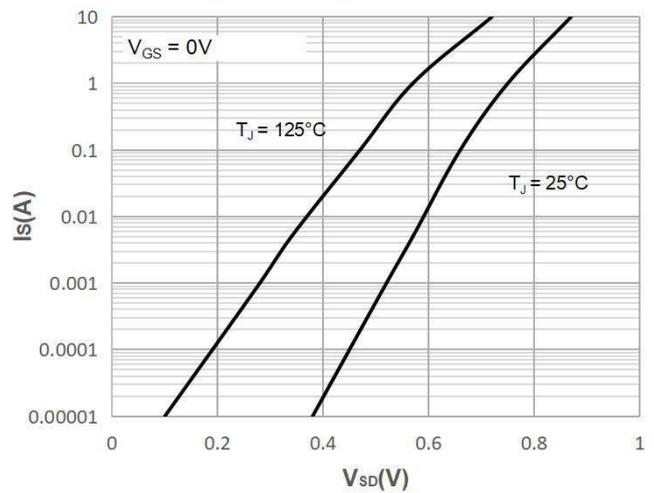


Figure 5: Gate Charge Characteristics

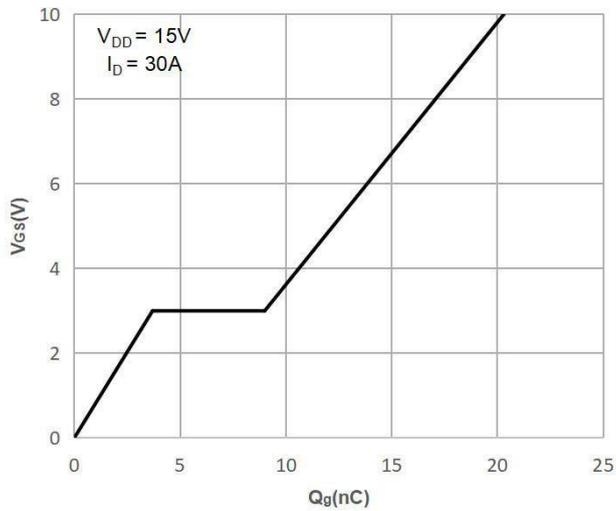
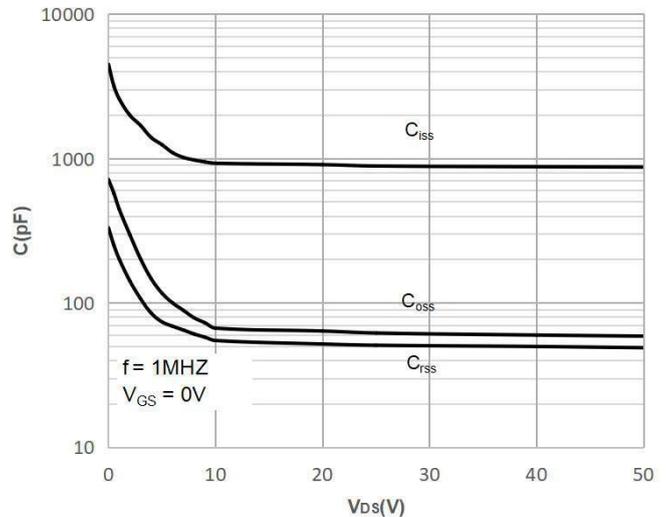


Figure 6: Capacitance Characteristics



## Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

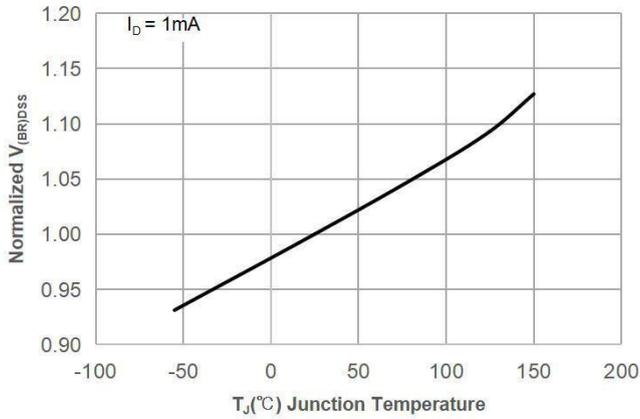


Figure 8: Normalized on Resistance vs. Junction Temperature

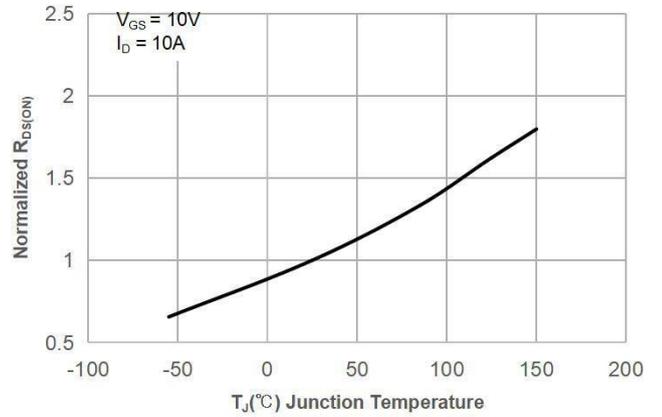


Figure 9: Maximum Safe Operating Area

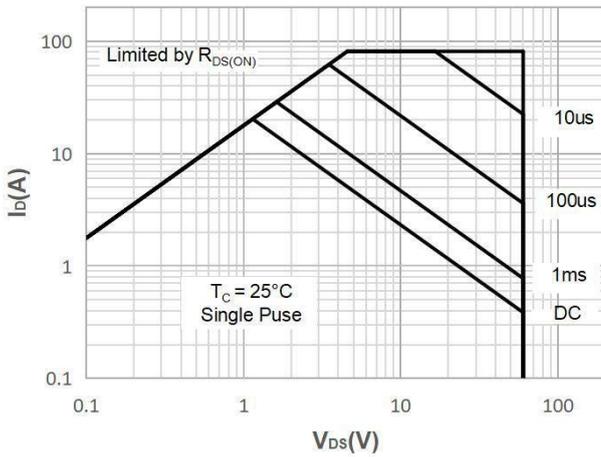


Figure 10: Maximum Continuous Drianc Current vs. Case Temperature

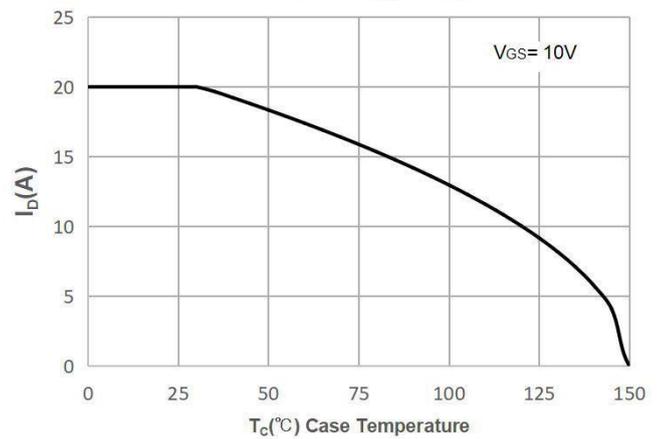


Figure 11: Normalized Maximum Transient Thermal Impedance

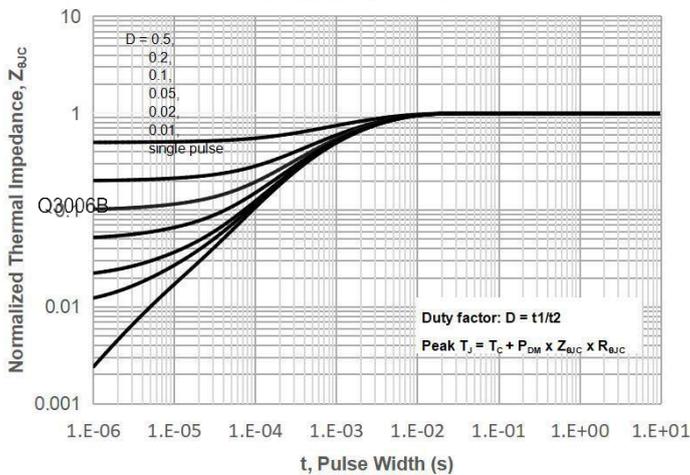
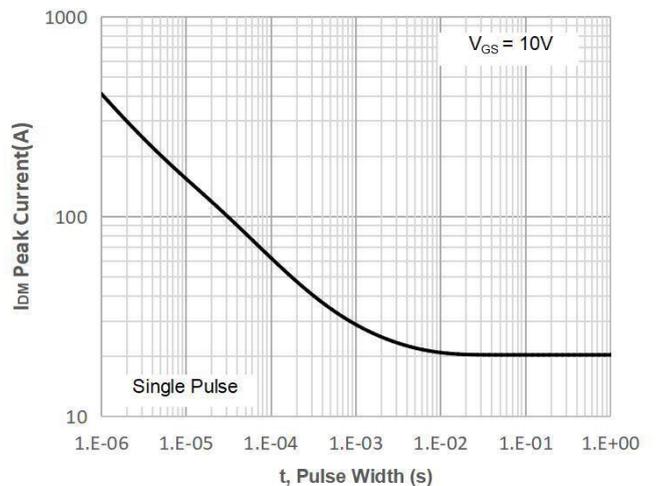


Figure 12: Peak Current Capacity



TestCircuit

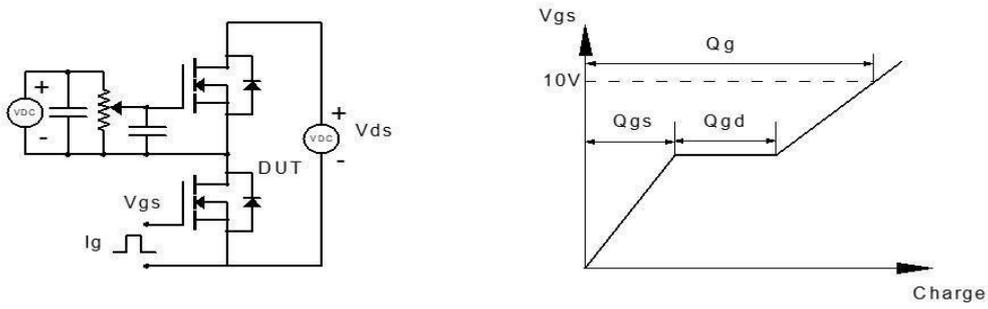


Figure 1: Gate Charge Test Circuit & Waveform

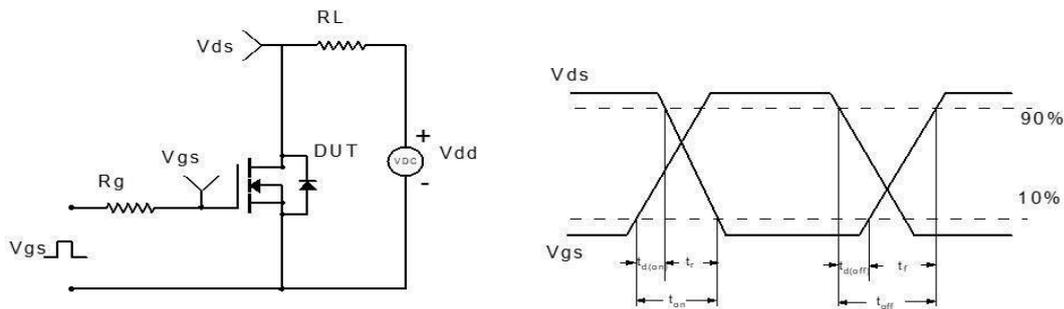


Figure 2: Resistive Switching Test Circuit & Waveform

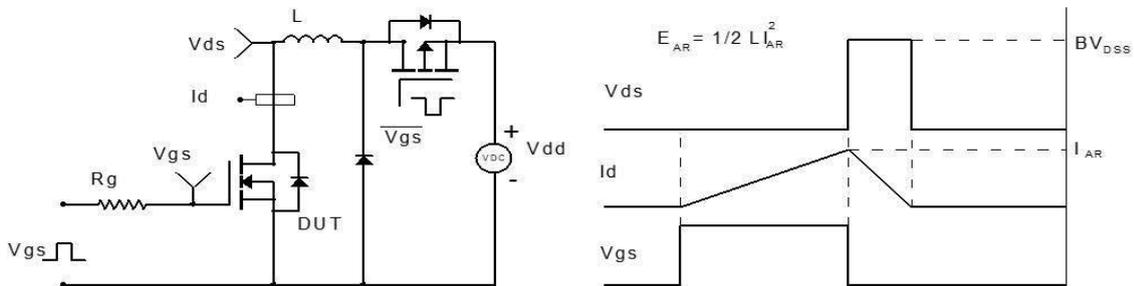


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

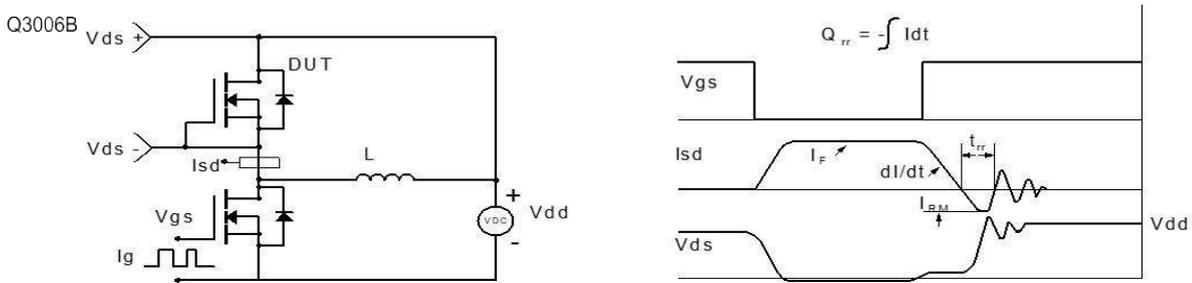
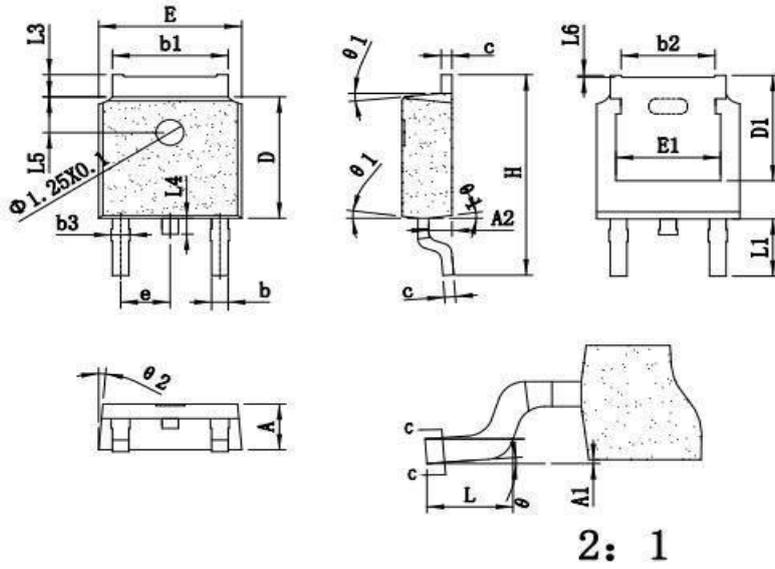


Figure 4: Diode Recovery Test Circuit & Waveform

**Package Mechanical Data(TO-252-3L)**



SYMBOL	mm		
	MIN	NOM	MAX
*A	2.20	2.30	2.38
*A1	0.00	—	0.15
*A2	0.90	1.00	1.10
*b	0.72	0.78	0.85
b1	5.23	5.33	5.46
b2	4.05	4.20	4.35
*b3	0.78	0.85	0.90
*c	0.47	0.52	0.55
*D	6.00	6.10	6.20
D1	5.40REF		
*E	6.50	6.60	6.70
E1	4.70	4.83	4.92
*e	2.286BSC		
*H	9.90	10.10	10.20
*L	1.40	1.55	1.70
L1	2.90REF		
L3	0.90	—	1.20
L4	0.75	0.85	0.95
L5	1.70	1.80	1.90
L6	0.00	0.06	0.12
* $\theta$	0°	—	5°
$\theta_1$	5°	7°	9°
$\theta_2$	5°	7°	9°

2: 1